Design of a High Power Density Inverter and FOC Implementation for UAVs

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Abstract—**Even nowadays, still some small huts in the alps need a helicopter to provide them with the necessities for living. This task is always connected with high costs and organisational effort. With the ongoing development in the field of unmanned aerial vehicles (UAVs) already a drone exist which can take over this task. Currently, this drone is limited to a payload of 100** kg**. In this paper, the design and optimisation of a 19.5** kW **inverter based on half-bridge configuration using Silicon Carbide (SiC) technology for this type of cargo drones is presented. The 1200** V**, 16** $m\Omega$ **SiC half-bridge modules of Wolfspeed provide the base for the power stage. With a switching frequency of 25** kHz **and a power density of 8.2876** kW/dm^3 **and 19.5** kW/kg **the system achieves several advantages for this use-case. In addition, the layout of the Printed Circuit Boards (PCB's) is optimised for altitudes over 3500** m**. In terms of control strategy, a Field Oriented Control (FOC) implementation on an ST microcontroller is performed. The system is optimised to work with a 19.5** kW **Permanent Magnet Synchronous Motor (PMSM) of MAD Components. For validation of the functionality, several tests are performed including double-pulse tests, tests on a passive RL load as well as tests with a Motor test bench including the selected PMSM and a torque sensor The measured system efficiency of the inverter and PMSM combination reaches 87.15** %**. The inverter itself reaches a peak efficiency of 98.42** %**. Further tests on the real drone are intended to be performed, and further optimisation will be done to allow a serial production of this design.**

Index Terms—**Inverter, SiC, UAV, Power Electronics, FOC**

I. INTRODUCTION

UAV'S, or more specific in this case cargo drones, can provide a cheap and efficient alternative to several tasks, e.g. delivering necessities to small huts high up in the mountains. Especially for these companies, it is of major interest to have a high performance, but also light weight motor drive. A previous work is done in article Design and Demonstration of High Power Density Inverter for Aircraft Applications ([1]). This paper describes a design methodology for such a high power density converter and considers different typologies and power devices. For verification purposes, a 50 kVA three-phase power inverter is designed and evaluated as an example. This implemented inverter has a switching frequency of 65 kHz and can reach an efficiency of 97.77 %. In the article Design of a Fast Switching 200 kVA Silicon-Carbide (SiC) Drive Inverter for Aviation Application ([2]) a 200 kVA SiC drive inverter is shown. This SiC drive inverter reaches a power density of 89 $\frac{\text{kW}}{\text{dm}^3}$ and 79 $\frac{\text{kW}}{\text{kg}}$ with a measured peak efficiency of 98.8 % at a switching frequency of 48 kHz. For evaluation of the designed inverter in this specific use-case, a comparison to an existing inverter of the MAD AMPX FOC 60A FOC60A of MAD Components, which is recommended for the used motor, is done. This design is intended to fulfil several requirements, including creepage distance of 12.5 mm for high voltage areas (IPC-2221B) for uncoated external conductors, weight under 1 kg CAN communication and own internal power supply for electronics, 3.3 V and 12 V. Table I shows the main parameters of interest for this design.

Parameter	Value
V_{bus}	400 V
I_{DC}	49.1 A
P_{out}	19.5 kW
I_{outp}	64 A (peak)
f_{sw}	25 kHz

II. METHODS

A. MECHANICAL DESIGN

When mounted on the drone, the inverter will be exposed to vibrations, low temperatures, high humidity or even rain. To handle this conditions, a well-designed sealed housing is needed. Figure 1 shows a first reference design of two inverters mounted on a drone arm. The placement of the inverter in this location provides forced air cooling for the system by the propellers.
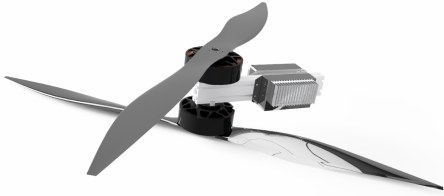

Fig. 1. CAD model of the mechanical design mounted on one arm of the drone.

For handling humidity and temperature inside the housing, it is possible to install an additional PWM controlled fan and NTC inside the housing. Especially at low temperatures, the circulating air can be used to prevent condensation on the PCBs and components and a controlled environment is given. Furthermore, additional coating of the PCBs is in discussion for the 2nd generation of this inverter. A thermal simulation in Ansys Icepak for better understanding of the cooling concept is done in the thesis to this paper [3].

Figure 2 shows an exploded view of the design for first tests. Of special interest are the 3D-printed spacers located on the left and right, which guarantee the correct placement of the single PCBs and function as an additional electrical isolation in terms of air distance between the housing and the inverter. The SiC half-bridge modules are mounted on the heatsink with a defined pattern of heatpaste according to the application note of Wolfspeed to guarantee a good distribution over the whole surface. For additional mechanical stiffness and protection of the Press-Fit connectors, each half-bridge module is screwed to the DC-Link PCB additionally on the top-side. [4]
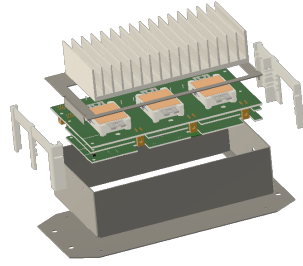

Fig. 2. Exploded view of inverter housing.

B. PCB Design

The designed inverter consists of a stack-up of three PCBs. This allows a clear separation of different voltage levels. In addition, it fulfils the size requirements given by the customer.

1) DC-LINK PCB: This PCB works as the power stage of the inverter. On this the CAB016M12FM3 SiC half-bridge modules of Wolfspeed, Würth Electronics Redcube (7461101) connectors for power including DC input from the battery pack as well as AC output to the PMSM are located. Also, the DC-Link capacitance and differential hall sensors for current measurement of the three phases are placed on this PCB. The DC-Link capacitance consists of a combination of 11 5.6 μF C4AQLBU4560A1WK

of Kemet as the main capacitance and three $1\,\mu F$ CeraLink B58031I5105M062 of TDK located the nearest possible to the power terminals of the half-bridge modules. To keep a low profile, the TLI4971A120 differential hall sensors of Infineon are used to measure the phase currents. Figure 3 shows a 3D model of the designed PCB.

As can be seen, a strict separation between the different regions is performed. These regions are the DC input, the AC output as well as the signal part. This signal part includes the analogue output of the current measurements as well as the output of the in the modules, integrated NTCs. To handle the expected currents, of $64\,A$ peak on the AC terminals and $49.1\,A$ on the DC, a 4 layer design is used with a minimum copper thickness of $70\,\mu m$. Big planes and random vias as well as stitched vias around high power connections allow a sufficient current distribution throughout the regions.

In addition, cut-outs are located throughout the board to provide the necessary creepage distance for altitudes over $3500\,m$.
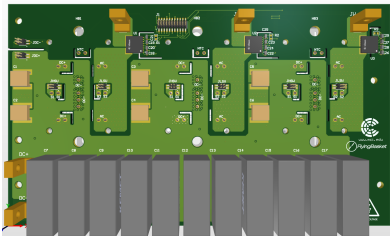

Fig. 3. Top view of DC-Link PCB.

2) DRIVER PCB: Due to limitations in dimension, the driver circuitry is located on a separated PCB, the Driver PCB. By using connectors, a short connection to the Gate and Kelvin Source terminals of the half-bridge modules can be guaranteed.

Figure 4 shows the top view of the 3D design done in Altium. On the top left, a connection of the DC-Link Voltage including the inductive part of an CLC filter is shown. This connection is needed for the voltage measurement as well as the internal supply, which will be discussed in the control PCB section.

On the lower part the Drivers are located with separation of low voltage and high voltage region. The low voltage region on the bottom is used for the PWM signals, driver enable signals, as well as the power supplies coming from the control PCB.
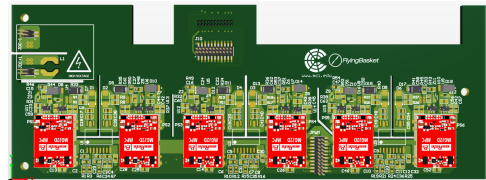

Fig. 4. Top view of the Driver PCB.

Of special interest on this four layer $1.55\,mm$ $35\,\mu m$ PCB is the layout of the driver region. Figure 5 shows the layout of the layers for the driver circuitry of phase W. The bottom part in this figure shows the low voltage region, mentioned before.

To guarantee again the required creepage distance, cutouts are located between the analogue part on the bottom and between high and low side of the gate driver. The selected half-bridge driver Si823H2CD, see detail 3 in figure 5, of Skyworks Solutions itself provides an $5\,kV$ insulation as well as several protection functions. These functions are a minimum dead time protection, short circuit protection and under-voltage lockout.

For the layout of the high voltage switching region, a symmetrical approach is selected to provide the same inductance path for high and low side SiC MOSFET, see detail 5 in figure 5. Each MOSFET, or driver side, is provided with an own isolated unreg-

ulated power supply, type MGJ2D121505MPC-R7, of Murata Power Solutions which provides voltage levels of 15 V for turn-on and −5 V for turn-off, see detail 4 in figure 5. Detail 1 in figure 5 shows the top layer plane used for supply of the unregulated DCDC converters. In addition, for stabilisation of this unregulated power supply low-dropout regulators (LDO's) are used, detail 6 in figure 5. For EMI reasons on the second layer, see detail 2 in figure 5, ground planes are located. On the PWM input side this corresponds to the signal ground while on the PWM output, secondary side, the Kelvin Source of the individual MOSFET is used for this purpose.
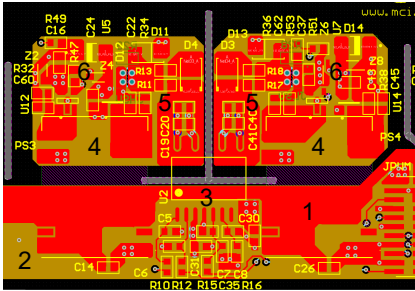

Fig. 5. Detailed view of layer design for driver of phase W.

3) CONTROL PCB: Figure 6 shows the top-view of the control PCB done in Altium. On the left top, the circuitry for the internal supply is located. By using a Viper26LN off-line converter, a buck converter is implemented [5]. This buck converter regulates down the DC-Link voltage from 400 V to 18 V DC, which then again is being regulated to 12 V and 3.3 V using additional DCDC converters and LDOs.

In this high voltage region also a Si923B-IS of Skyworks Solutions isolated amplifier for voltage measurement is located. By the use of a voltage divider, thin-film resistors with a tolerance of 1 % and a temperature coefficient of resistance (T.C.R) of ±100 ppm/°C, the nominal input for this amplifier

can be achieved.

In the middle, operational amplifiers for signal conditioning of the current sensor signal and NTCs are placed. This operational amplifier circuitry provides the analogue signal for the ADCs of the MCU and is designed following the guidelines in [6].
To allow a flexible change of the MCU a SiBrain dotted board of Mikroe is used, currently a with a STM32F746ZG mounted, which provides the CAN interface for communication with the flight controller of the drone as well as the PWM signals for the inverter and is the main control in the design. For communication and debugging, in addition, a JTAG and SWD interface is implemented. For testing ADC measurements, a DAC output is also provided, which can be used also for debugging and testing purposes.

On the right side, status LEDs and a thermocouple amplifier for possible measurement of Motor temperature is placed.
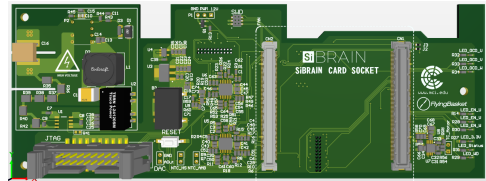

Fig. 6. Top view of the Control PCB.

C. FIRST PROTOTYPE

Figure 7 shows the first assembled prototype of this series. For measurement and testing purposes, some modifications are done. This includes twisted cables for measurement of Gate and Source directly connected to the MOSFETs and lifted inductance of the buck converter for current measurement of supply. In addition, by means of dismounting of one DCDC-Converter, a separation of 12 V and 3.3 V auxiliary supply was done for testing purposes. For programming and debugging purposes, a STLINK V3SET debugger is connected via the JTAG interface.
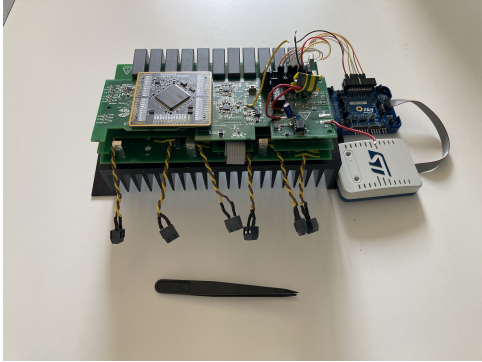
Fig. 7. First fully assembled prototype.

D. SOFTWARE

In this section, a description of the implemented software is given. Figure 8 shows the main system architecture implemented on a STM32F746ZG of STMicroelectronics. The used control strategy for this implementation is sensor-less FOC. By the use of a Back EMF Observer, the motor speed as well as the rotor phase is estimated. For this purpose, a mathematical model of the selected M50C35 PRO EEE 9KV of MAD components is implemented. Two internal state machines are used for proper control of the system. The overall system is controlled by the global state machine. In this state machine four different states exist, fault state, stop state, ready state and run state. For the control of the inverter itself an additional state machine, called inverter state machine, is implemented and works as a subsystem of the global state machine.

In this state machines, several functionalities are implemented [7]. Starting from the system initialisation where the timers get configured and variables are preset, e.g. level of under-voltage error. After this, an ADC calibration for the current measurement is done. Then the global state machine is started and is used to manage the overall system including enable and disable of PWM. With an internal global

command generation the values of interest, including DC-Voltage, phase currents, temperature of the modules and heatsink and estimated RPM of the motor, get read-out in an $40\,\mu s$ interval. Over-voltage as well as over-current are triggered separately with an interrupt function to provide a fast and reliable turn-off. The implemented software includes four different control strategies including torque control with FOC, speed control with FOC, Volts per Hertz control and Ampere per Hertz control. The main algorithm used is the torque control with FOC. By the use of command words, the space vector PWM generation can be started.
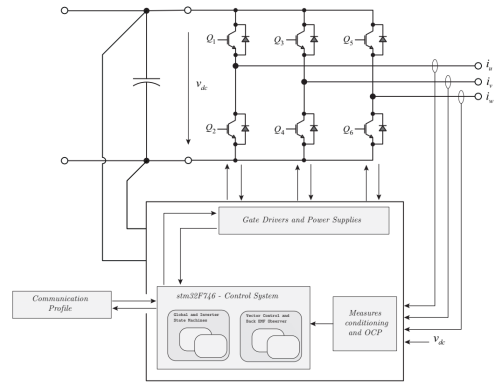

Fig. 8. Principle system architecture [8].

E. TEST SETUP

To provide a safe testing environment, especially at higher voltages and loads, different setups and considerations are made. Figure 9 shows the implemented testing box where a safe testing of the prototype can be performed. As in malfunction even an explosion of the half-bridge modules is possible, it consists of $10\,mm$ thick Plexiglas plates with several cutouts for measurement and cooling purposes. It includes the possibilities for mounting fans to provide active cooling to the system, which is also given on the real drone.
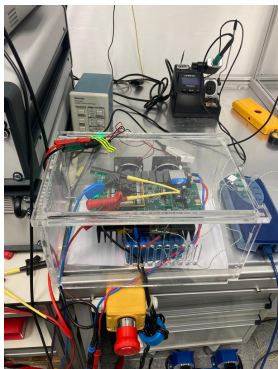
Fig. 9. Testing box for safety reasons.

To perform the necessary tests, especially on the real motor, a motor test bench is set up with the corresponding hardware, including two M50C35 PMSM of MAD components and a TS111 torque sensor of Magtrol. Figure 10 shows this motor test bench. The mounted motor on the left serves as the main motor for testing the inverter. To provide load to the system, a second motor can be mounted on the right and is then used in the generator load, where the phases will be connected to a resistive load. With the torque sensor located in the middle, a measurement of the applied torque is provided.
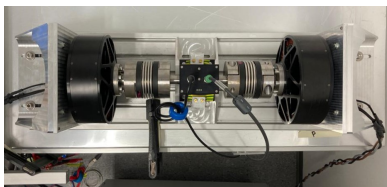

Fig. 10. Motor test bench with torque sensor and motor mounted.

Figure 11 shows the used power supplies. As a power supply, two GEN300-17-3P208 of TDK are used. This power supply can provide up to $300\,\text{V}$ output voltage and $17\,\text{A}$ output current each. With two power supplies in parallel, a maximum reachable power of $10.2\,\text{kW}$ is given. By using them

in series, the rated $400\,\text{V}$ of the inverter can be reached with a maximum power of $6.8\,\text{kW}$. On top of these, a InfiniiVision DSOX2014A oscilloscope of Keysight is located. For supplying the fans and control electronics external during debugging, an additional laboratory power supply is used.
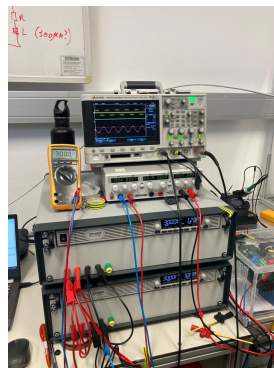

Fig. 11. GEN300-17-3P208 of TDK power supplies and InfiniiVision DSOX2014A oscilloscope of Keysight.

III. RESULTS

To guarantee an efficient measurement procedure, a test-plan is set up. This test-plan includes tests of the single PCBs, e.g. test of the Viper26, internal buck converter and check of driver functionality. The main tests including double-pulse tests, tests on a passive RL load and tests on the real motor are shown in the following.

A. DOUBLE-PULSE TEST

For this test, the high-side of the half-bridge is being short-circuited with an $125\,\mu\text{H}$ inductance and the low side is being switched with two pulses. The DC-Link voltage in this test is the nominal $400\,\text{V}$. To avoid too much current on the internal MOSFET diode, in addition also the high-side is being switched complimentary with a dead-time of $1\,\mu\text{s}$. This dead-time will be reduced to increase the system efficiency. The pulse time for the first pulse

is chosen to be, 15 μs and for the second pulse, a pulse time of 5 μs is used. By using the known relationship between current and voltage inside a conductor, Equation 1, the maximum reached current can be calculated to be 64 A after the second pulse. For the measurement, differential probes of Ridley engineering with a bandwidth of 30 MHz and a Tektronix TCPA300 AC/DC current probe amplifier with a TC312A current probe is used with a InfiniiVision DSOX2014A oscilloscope of Keysight. Figure 12 shows this double-pulse test.
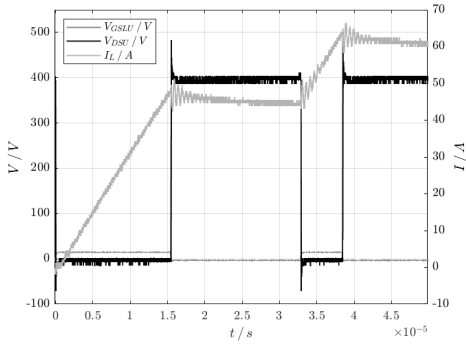

Fig. 12. 400 V double-pulse test with 125 μH inductance.

In the following, the results of this double-pulse test are investigated in deeper details. With this measurement set up a maximum overshoot of 99.52 V, 24.8 % of nominal voltage, is given after turn-off of the second pulse. The rise-time, from 90% nominal voltage to 10% of V_{DSU}, is measured to be 19 ns. This means that the $\frac{dv}{dt}$, the change of voltage over time, during turn-on is 21.05 $\frac{V}{ns}$ and the change of current over time $\frac{di}{dt}$ corresponds to 2.66 $\frac{A}{ns}$. The fall-time t_f is measured the same way as the rise-time, t_r with the difference that the turn-off occurs at the nominal current of 64 A. It corresponds to 13 ns and therefore an $\frac{dv}{dt}$ of 30.79 $\frac{V}{ns}$ and an $\frac{di}{dt}$ of 4.92 $\frac{A}{ns}$ is being calculated. Deeper investigation is done in the thesis to this paper [3].

$$V_L = L\frac{di}{dt} \tag{1}$$

B. Passive RL load

1) Thermal calibration: For better understanding of the generated losses inside the inverter, a thermal calibration is done. For this purpose, a reversed voltage is applied to the DC terminals. This allows that the structurally given body diode inside the MOSFETs are used and losses can be generated. With a temperature measurement using type K thermocouples with a TC-08 logger of Picotech. For this purpose, small holes are drilled in the heatsink directly underneath the three half-bridge modules. Figure 13 shows the result of this thermal calibration with forced air cooling. This results can now be used to validate the MOSFET losses in dependence of the heatsink temperature.
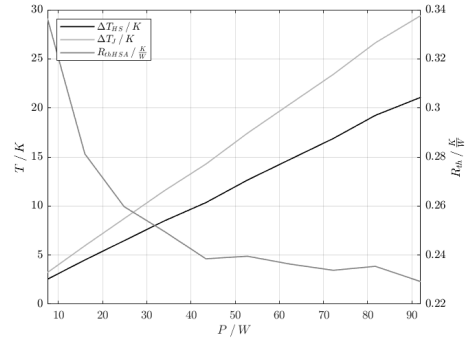

Fig. 13. Result of thermal calibration.

2) Results: Here, the results of the inverter test with a passive RL Load is presented. For this purpose, a 4 Ohm 500 μH passive RL load is used. Figure 14 shows the phase to phase voltage, $V_{UVph-ph}$ which is measured using differential isolation probes of Ridley engineering. This test is performed using the current control at a direct current reference i_{Sdref} of 33 % of the nominal current, or 21.12 A peak.
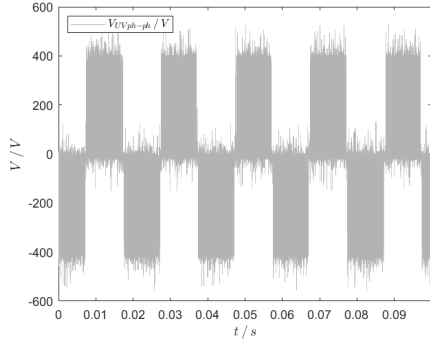
Fig. 14. Phase to phase voltage V_{Uph-ph} of phase U during passive RL load test in current control.

Fig. 16. Efficiency of different working points on the RL load.

Figure 15 shows the current waveform, measured directly on the phase output using current probes of Tektronix, type TCP312A. As can be seen, the main frequency of the current is at 50 Hz, which is the set point for the current control. By the use of a PPA3500 power analyser of N4L and IT205-S current sensors of LEM the inverter efficiency is measured. The results of this measurement are shown in figure 16. A peak efficiency of 98.42 % is reached at an output power of 5.34 kW.
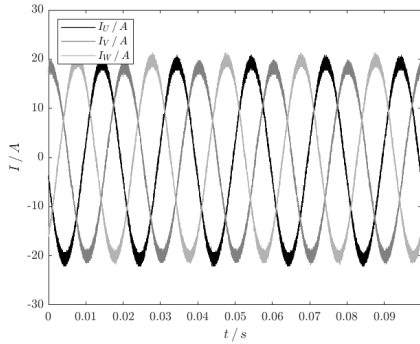
C. Tests on real motor

In this section the results of the closed loop torque control at 30 % of nominal torque, $T = 19.2$ Nm, is shown. As a load in this test for the second motor used in generator mode, a $2\,\Omega$ resistance is chosen. Figure 17 shows the inverter output current I_{Uinv} of phase U and I_{Vinv} of phase V. The electrical frequency f_{elec} is equal to, $f_{elec} = 1092.57$ Hz which corresponds to a rotational speed $\omega = 2185.15$ RPM.
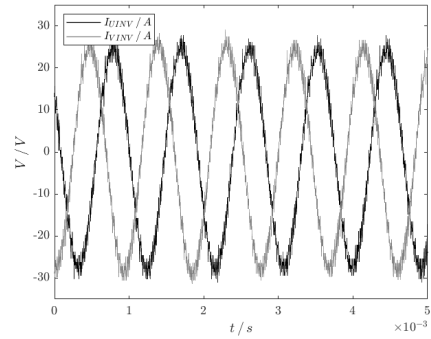

Fig. 15. Phase current I_U, I_V and I_W during passive RL load test in current control.

Fig. 17. Inverter phase currents I_{Uinv} and I_{Vinv} during real motor test at 30 % torque reference.

Figure 18 shows a contour plot of the system

efficiency η_{sys}, including the inverter and PMSM motor, in dependence of the rotational speed w and the motor torque T. A peak system efficiency of $87.147\,\%$ is recorded.
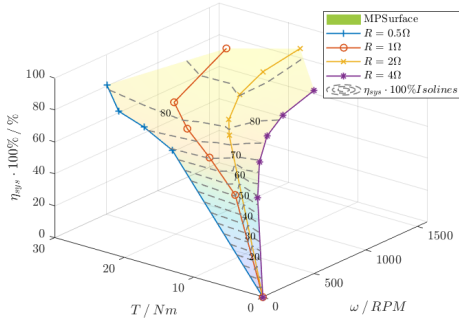

Fig. 18. 3D plot of system Efficiency versus torque T and rotational speed ω of the implemented inverter.

IV. CONCLUSION AND OUTLOOK

In this paper, a $19.5\,\text{kW}$ three-phase inverter design for a real UAV application is presented. A first prototype is designed, assembled and tested. First tests including start-up of the single PCB's as well as double-pulse tests on the whole inverter are done. The results of this are as expected. Further tests on a passive RL load and on a real motor are performed, and the nominal current is reached. A peak inverter efficiency of $98.42\,\%$ and a peak system efficiency of $87.15\,\%$ are measured.

As a next step, tests at higher power levels, up to $10.5\,\text{kW}$ input power, will be done. The inverter is then used with the real drone for further testing up to the nominal power. With this information and the feedback of the customer, a second generation of the presented inverter with optimised layout and design can be achieved.

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